Amendments to the Claims

1. (currently amended) A quantum device, comprising:

an electrically inert solid substrate within which there is;

a charge qubit comprising a pair of dopant atoms having a net charge and an electric field having two potential wells, wherein the two potential wells are located adjacent respective dopant atoms;

and wherein ~~the~~ a location of the net charge in the electric field having two potential wells defines ~~the~~ a logical state of the qubit;

and wherein a first gate is located over a potential barrier between the two potential wells to control barrier height; and[[,]]

at least one second gate is located to control relative shapes and sizes of the two potential wells, wherein the substrate is silicon, the dopant is phosphorus and the charge qubit is a P-P^{+} system and its electrical field having the two potential wells.

2. Cancelled..

3. (currently amended) A quantum device according to claim 1 ~~2~~, wherein the logical state of the charge qubit is defined by the location of a single electron in one of the two potential wells.

4. (currently amended) A quantum device according to claim 1 ~~2~~, wherein the the logical state of the charge qubit is defined by lowest symmetric or antisymmetric molecular states.

5. (currently amended) A quantum device according to claim 1 ~~2~~, wherein spacing between the P atoms is up to 200nm.

6. (original) A quantum device according to claim 5, wherein the spacing between the P atoms is in the range 20 to 100nm.

7. (currently amended) A quantum device according to claim 1 ~~2~~, wherein the two P atoms are buried to a depth in the substrate up to 200nm.

8. (previously presented) A quantum device according to claim 7, wherein the two P atoms are buried to a depth in the substrate in the range 5 to 50nm.

9. (currently amended) A quantum device according to claim 1 ~~2~~, wherein the silicon substrate is coated with an insulating layer ~~to isolate the donor electrons from any surface electrodes~~.

10. (original) A quantum device according to claim 9, wherein the insulating layer is SiO_2.

11. (currently amended) A quantum device according to claim 1 ~~2~~, wherein gate electrodes are placed on ~~the~~ a surface of the substrate above the donor atoms to allow for external control of charge wavefunctions, wherein the first gate is a 'barrier' gate or B-gate.

12. Cancelled.

13. (currently amended) A quantum device according to claim 11 ~~12~~, wherein the at least one second gate is a ~~known as the >potential off-set=,>symmetry= or S-gate~~ 'potential off-set',

'symmetry' or S-gate.

14. (original) A quantum device according to claim 13, wherein suitable biasing of the first and second gates allows one qubit logic operations to be performed.

15. (original) A quantum device according to claim 11, wherein one or more charge detection devices are provided on the surface of the substrate for qubit readout and to confirm initialization of qubits.

16. (original) A quantum device according to claim 15, wherein the charge detection device is a sensitive field-effect transistor, or a single electron transistor (SET).

17. (currently amended) A quantum device according to claim 1 ~~2~~, wherein a configuration comprising two dopant atoms, surface gates and surface charge detection devices[[,]] is repeated many times on a single silicon chip, allowing for scale-up to a many qubit processor.

18. (currently amended) A quantum device according to claim 17, wherein the device is cooled to ensure that the ~~donors~~ dopant atoms are not thermally ionised and to minimise coupling of the charge qubits to an environment.

19. (previously presented) A quantum device according to claim 18, wherein the device is cooled to 4K or below.

20-27 Cancelled.